United States Patent [19]

Haag et al.

[11] **4,455,624**

[45] **Jun. 19, 1984**

[54] **LOGIC STATE ANALYZER WITH FORMAT SPECIFICATION**

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[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **457,599**

[22] Filed: **Jan. 13, 1983**

Related U.S. Application Data

[60] Division of Ser. No. 210,462, Nov. 25, 1980, Pat. No. 4,373,193, which is a continuation of Ser. No. 75,787, Sep. 17, 1979, abandoned, which is a division of Ser. No. 828,138, Aug. 29, 1977.

[51] **Int. Cl.**[3] **G06F 3/14**; G06F 7/00

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 382/1

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 26,919	7/1970	Hagelbarger et al.	364/900
4,040,025	8/1977	Morrill, Jr.	364/900
4,100,532	7/1978	Farnbagh	382/1
4,161,031	7/1979	Olander et al.	364/900 X
4,250,562	2/1981	Haag et al.	364/900
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OTHER PUBLICATIONS

Operating and Service Manual Supplement-1611A OPT A68-Hewlett Packard-Part No. 10257-909-07-5/81.

Operating and Service Manual Supplement-1611A OPT A80-Hewlett Packard-Part No. 10258-909-05-8/80.

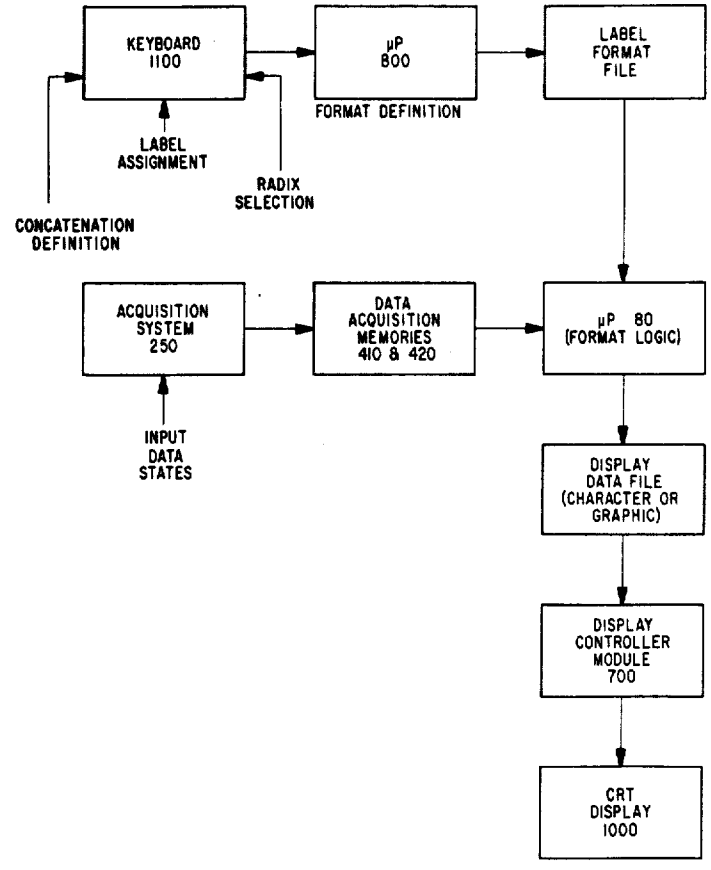
Primary Examiner—Harvey E. Springborn

Attorney, Agent, or Firm—Edward L. Miller

[57] **ABSTRACT**

Ongoing succession of states occurring in a collection of digital signals is monitored by a logic state analyzer which stores either all such states or a selected subset thereof meeting certain qualification criteria. The memory into which the states are stored is updated with oldest stored states being overwritten as the newest states are stored, the collectivity of which may be termed a captured trace. The above-mentioned qualification and sequential criteria are termed a trace specification. The utility of such a trace in a logic state analyzer is enhanced by allowing the user to divide the collection of digital signals into groups of related signals, assign symbolic labels to the groups, and indicate a radix for each group. Such division, assignment and indication may be termed a format specification. Subsequent trace specifications as well as the displayed or printed form of the trace itself then incorporate the format specification.

5 Claims, 16 Drawing Figures



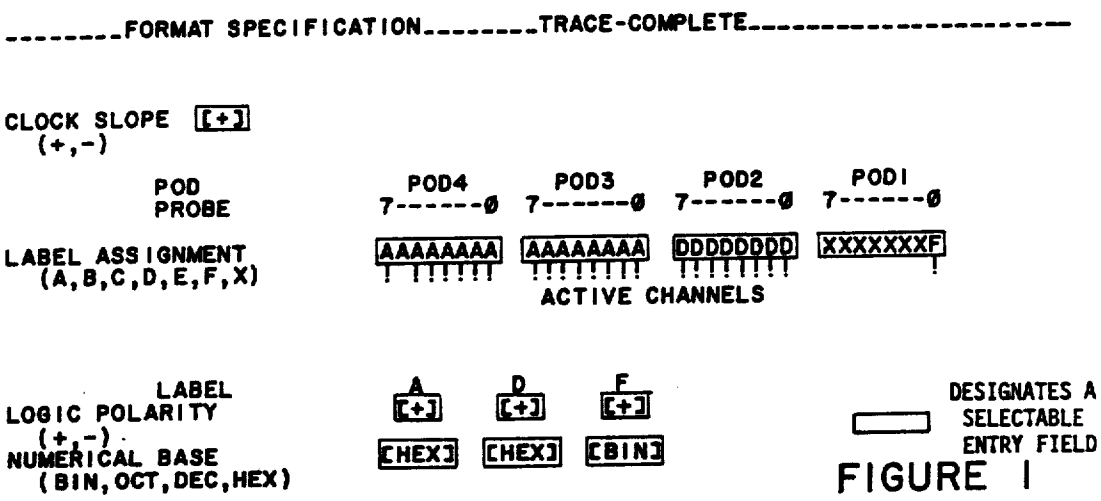


FIGURE 1

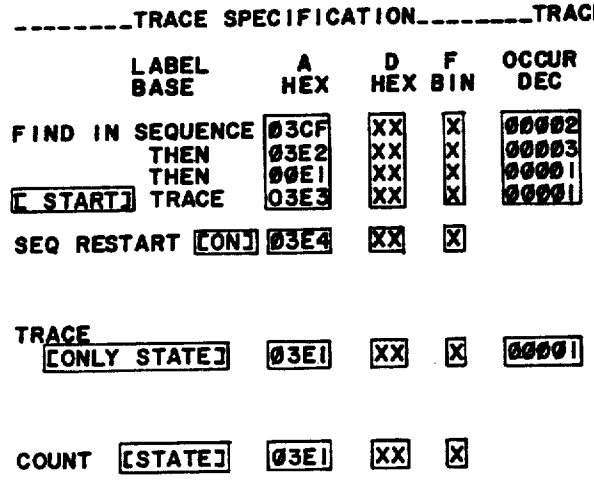


FIGURE 2

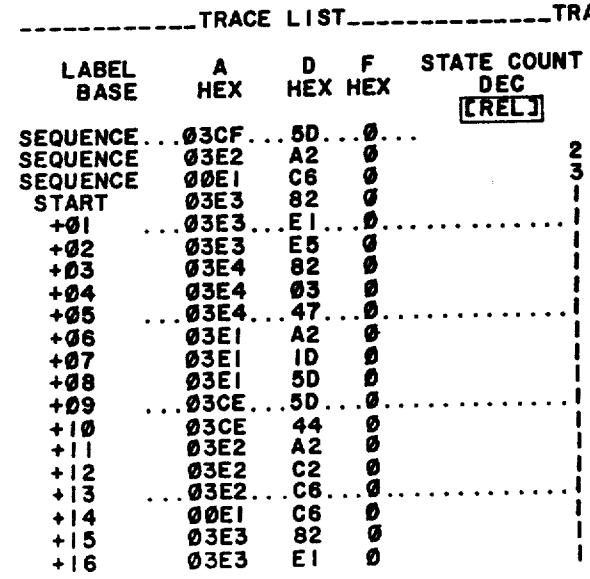


FIGURE 3

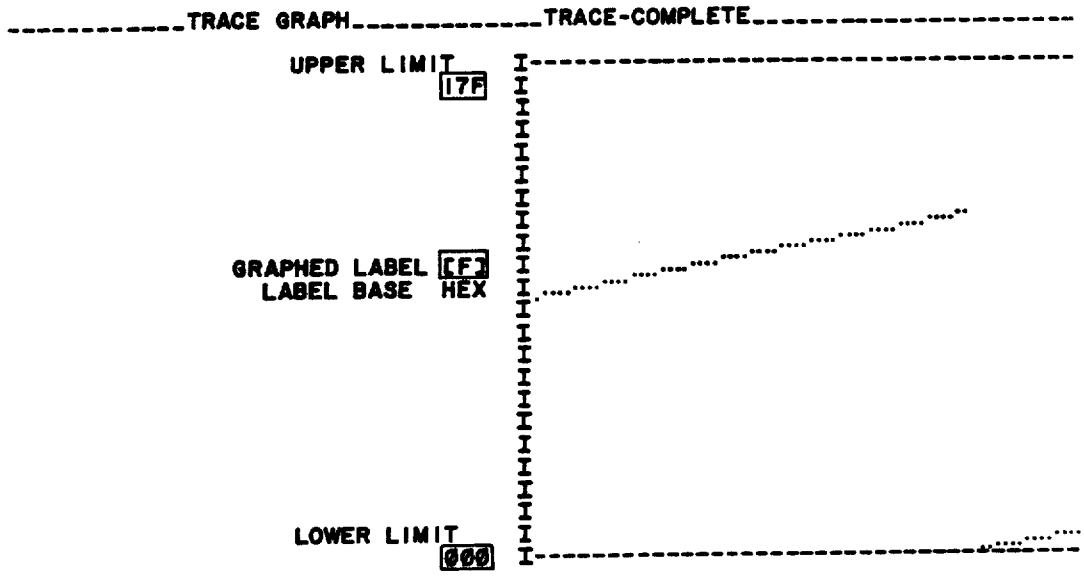


FIGURE 4

TRACE COMPARE — COMPARED TRACE-COMPLETE

LABEL BASE	A HEX	D HEX	F BIN	COMPARED TRACE MODE [STOP]
SEQUENCE	0000	00	0	
SEQUENCE	0000	00	0	
SEQUENCE	0000	00	0	
START	0000	00	0	
+01	0000	00	0	
+02	0000	00	0	
+03	0000	00	0	
+04	0000	00	0	
+05	0000	00	0	
+06	0000	00	0	
+07	0000	00	0	
+08	0000	00	0	
+09	0000	00	0	
+10	0000	00	0	
+11	0000	00	0	
+12	0000	00	0	
+13	0000	00	0	
+14	0000	00	0	
+15	0000	00	0	
+16	0000	00	0	

FIGURE 5

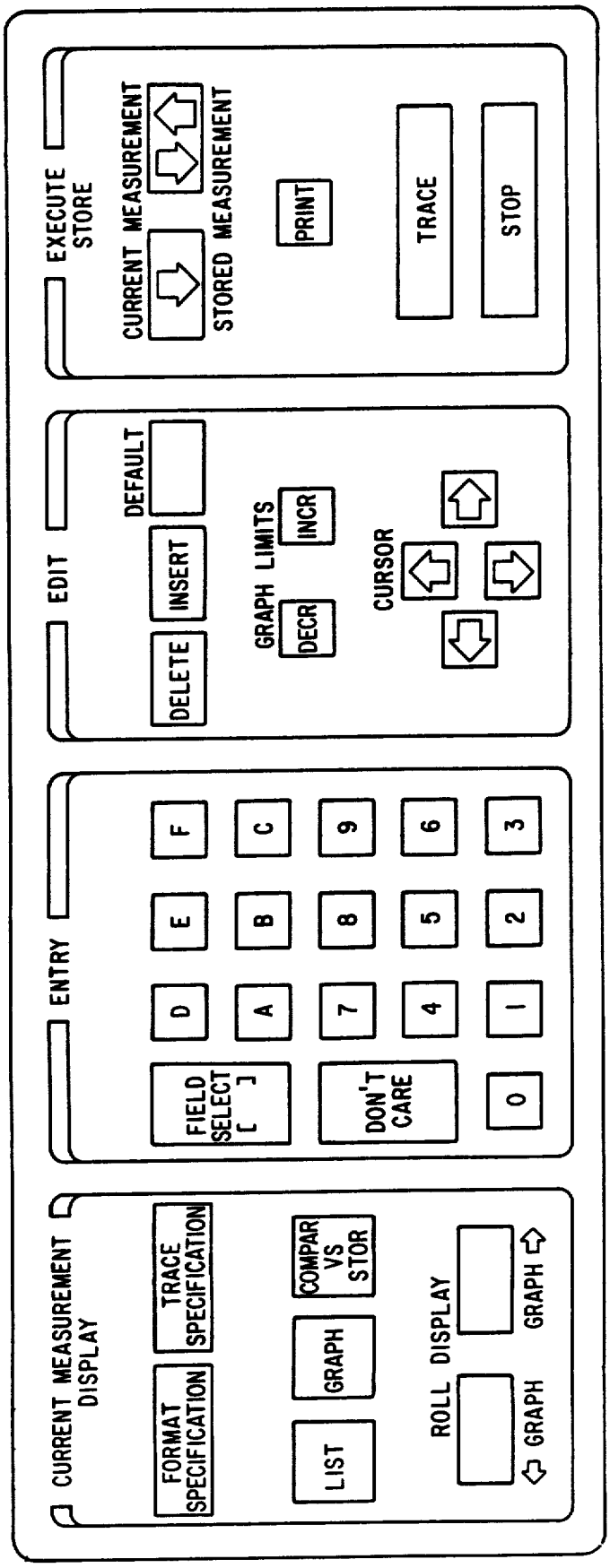

CURRENT MEASUREMENT DISPLAY
FORMAT SPECIFICATION
TRACE SPECIFICATION
LIST
GRAPH
COMPAR VS STOR
ROLL DISPLAY
GRAPH
GRAPH
ENTRY
FIELD SELECT [ ]
DON'T CARE
D
E
F
A
B
C
7
8
9
4
5
6
1
2
3
0
EDIT
DELETE
INSERT
DEFAULT
GRAPH LIMITS
DECR
INCR
CURSOR
EXECUTE STORE
CURRENT MEASUREMENT
STORED MEASUREMENT
PRINT
TRACE
STOP

FIGURE 6

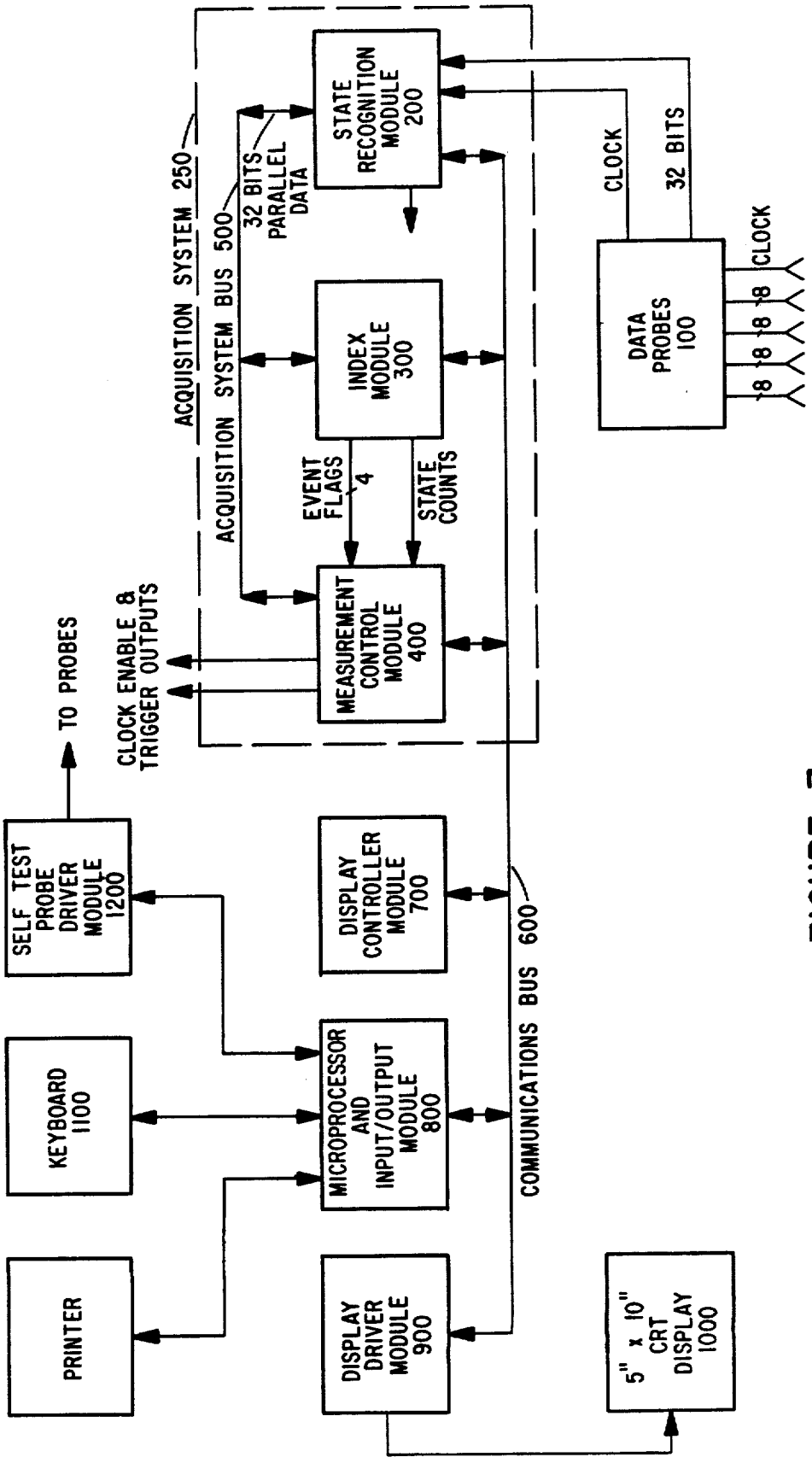

ACQUISITION SYSTEM 250
ACQUISITION SYSTEM BUS 500
32 BITS PARALLEL DATA
STATE RECOGNITION MODULE 200
INDEX MODULE 300
EVENT FLAGS 4
STATE COUNTS
MEASUREMENT CONTROL MODULE 400
CLOCK ENABLE & TRIGGER OUTPUTS
TO PROBES
CLOCK
32 BITS
DATA PROBES 100
8
8
8
8
CLOCK
SELF TEST PROBE DRIVER MODULE 1200
DISPLAY CONTROLLER MODULE 700
COMMUNICATIONS BUS 600
KEYBOARD 1100
MICROPROCESSOR AND INPUT/OUTPUT MODULE 800
PRINTER
DISPLAY DRIVER MODULE 900
5" x 10" CRT DISPLAY 1000

FIGURE 7

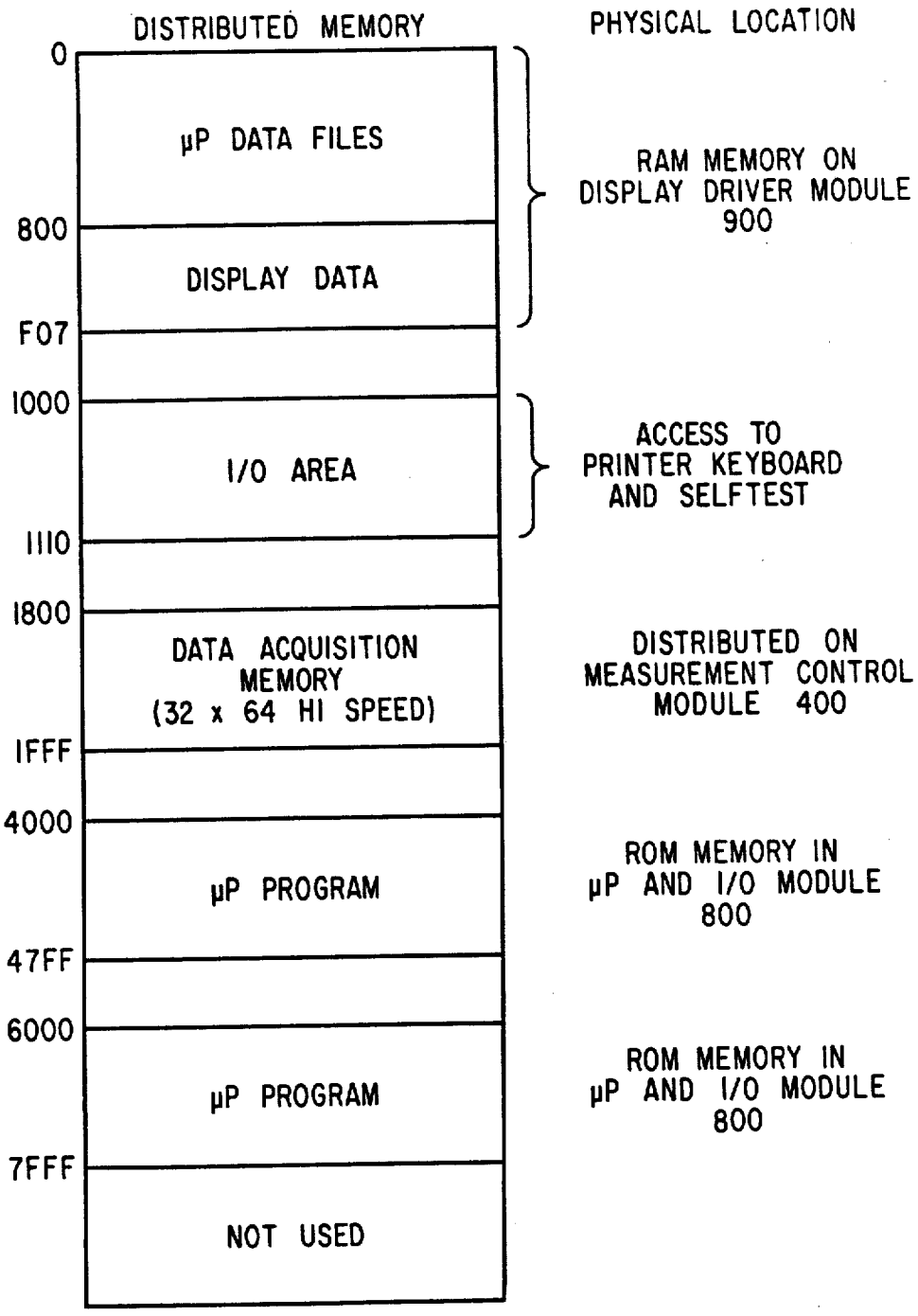

DISTRIBUTED MEMORY
PHYSICAL LOCATION
0
μP DATA FILES
800
DISPLAY DATA
F07
1000
I/O AREA
1110
1800
DATA ACQUISITION MEMORY (32 x 64 HI SPEED)
1FFF
4000
μP PROGRAM
47FF
6000
μP PROGRAM
7FFF
NOT USED
RAM MEMORY ON DISPLAY DRIVER MODULE 900
ACCESS TO PRINTER KEYBOARD AND SELFTEST
DISTRIBUTED ON MEASUREMENT CONTROL MODULE 400
ROM MEMORY IN μP AND I/O MODULE 800
ROM MEMORY IN μP AND I/O MODULE 800

FIGURE 8

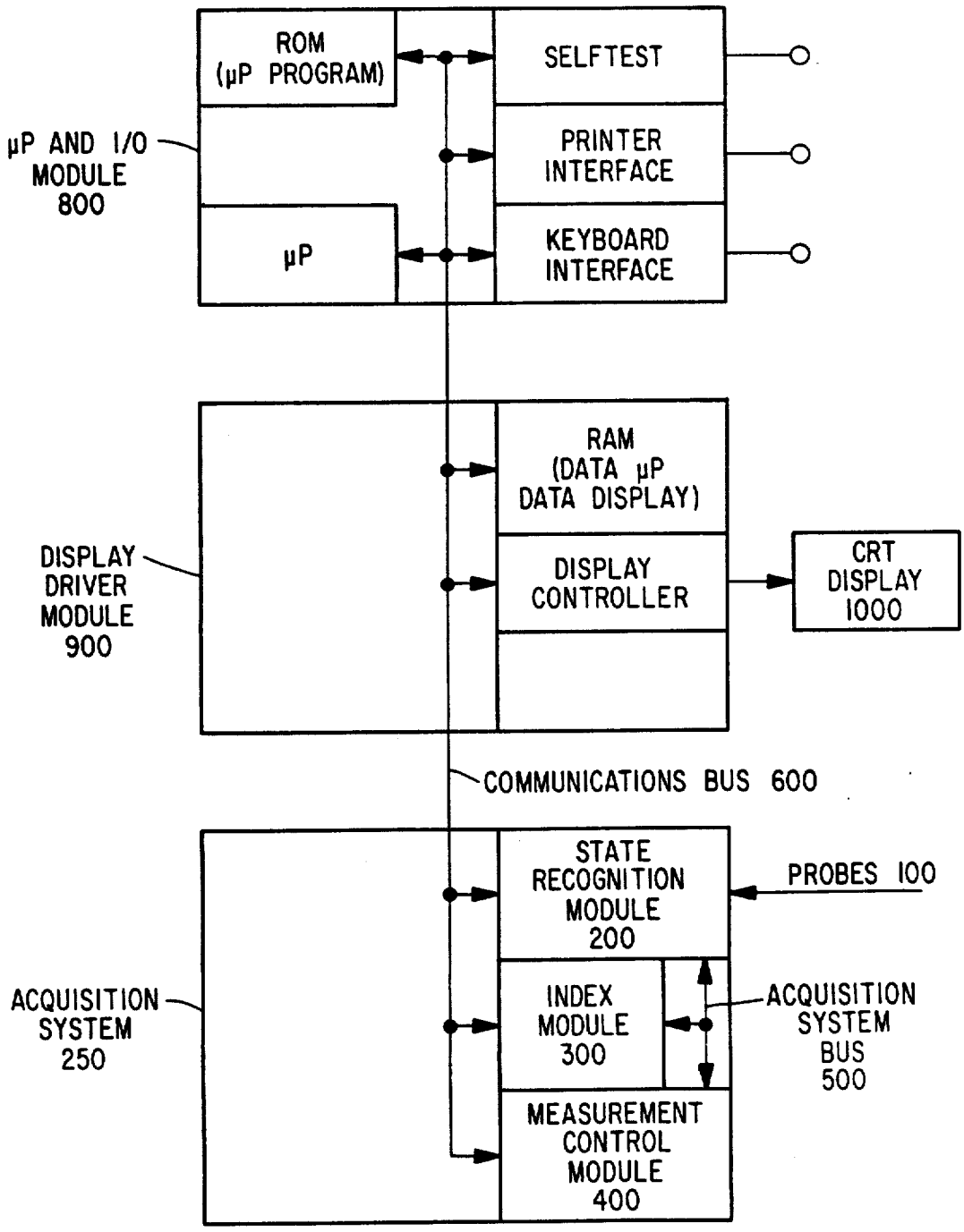

ROM
(μP PROGRAM)
SELFTEST
μP AND I/O
MODULE
800
PRINTER
INTERFACE
μP
KEYBOARD
INTERFACE
RAM
(DATA μP
DATA DISPLAY)
DISPLAY
DRIVER
MODULE
900
DISPLAY
CONTROLLER
CRT
DISPLAY
1000
COMMUNICATIONS BUS 600
STATE
RECOGNITION
MODULE
200
PROBES 100
ACQUISITION
SYSTEM
250
INDEX
MODULE
300
ACQUISITION
SYSTEM
BUS
500
MEASUREMENT
CONTROL
MODULE
400

FIGURE 9

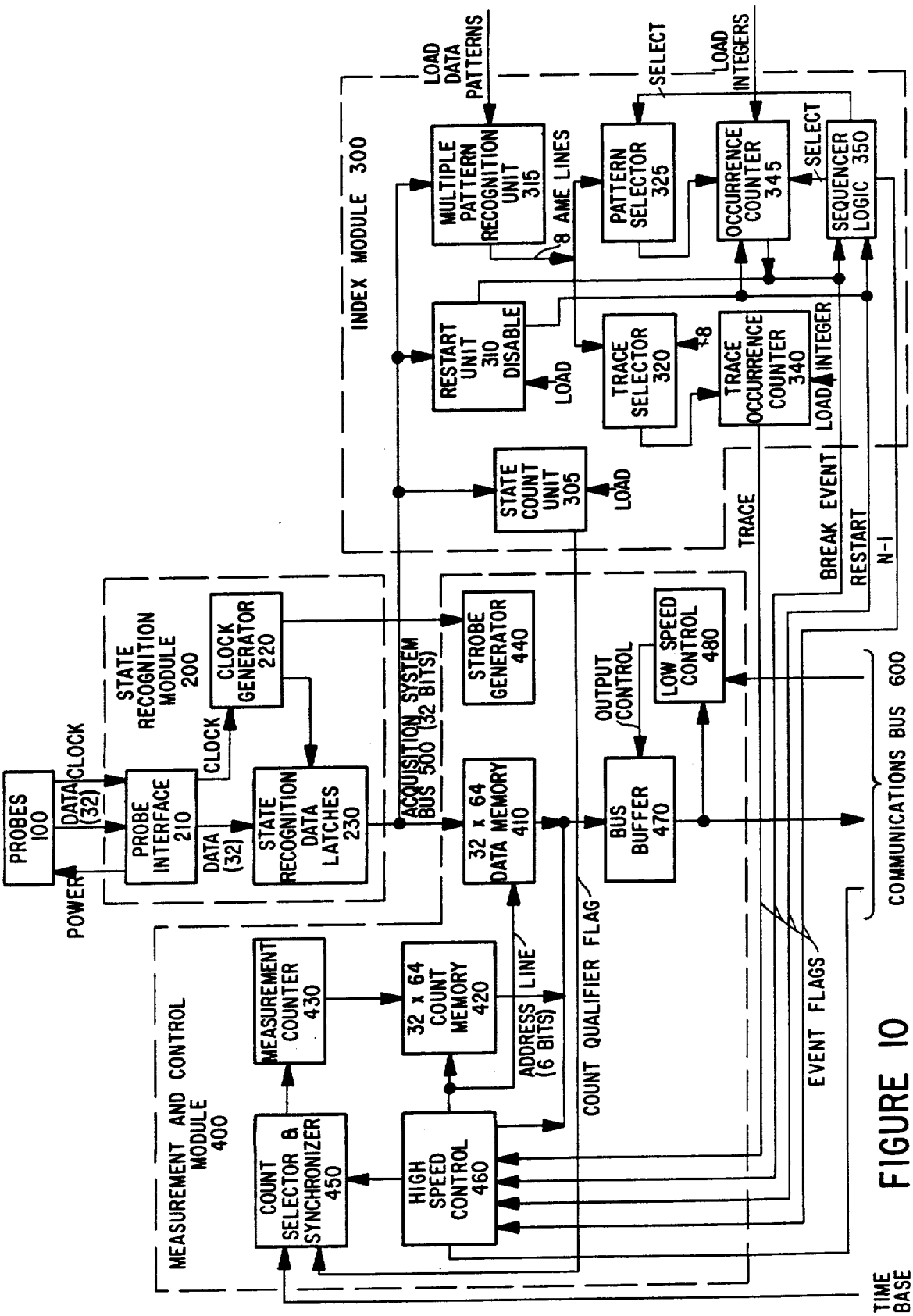

PROBES 100
POWER
DATA (32)
CLOCK
PROBE INTERFACE 210
DATA (32)
STATE RECOGNITION DATA LATCHES 230
STATE RECOGNITION MODULE 200
CLOCK
CLOCK GENERATOR 220
ACQUISITION SYSTEM BUS 500 (32 BITS)
STROBE GENERATOR 440
32 x 64 DATA MEMORY 410
BUS BUFFER 470
OUTPUT CONTROL
LOW SPEED CONTROL 480
COMMUNICATIONS BUS 600
INDEX MODULE 300
LOAD DATA PATTERNS
MULTIPLE PATTERN RECOGNITION UNIT 315
8 AME LINES
PATTERN SELECTOR 325
SELECT
LOAD INTEGERS
OCCURRENCE COUNTER 345
SELECT
SEQUENCER LOGIC 350
RESTART UNIT 310 DISABLE
LOAD
TRACE SELECTOR 320
8
TRACE OCCURRENCE COUNTER 340
LOAD INTEGER
STATE COUNT UNIT 305
LOAD
TRACE
BREAK EVENT
RESTART
N-1
MEASUREMENT AND CONTROL MODULE 400
MEASUREMENT COUNTER 430
32 x 64 COUNT MEMORY 420
ADDRESS LINE (6 BITS)
COUNT QUALIFIER FLAG
COUNT SELECTOR & SYNCHRONIZER 450
HIGH SPEED CONTROL 460
EVENT FLAGS
TIME BASE

FIGURE 10

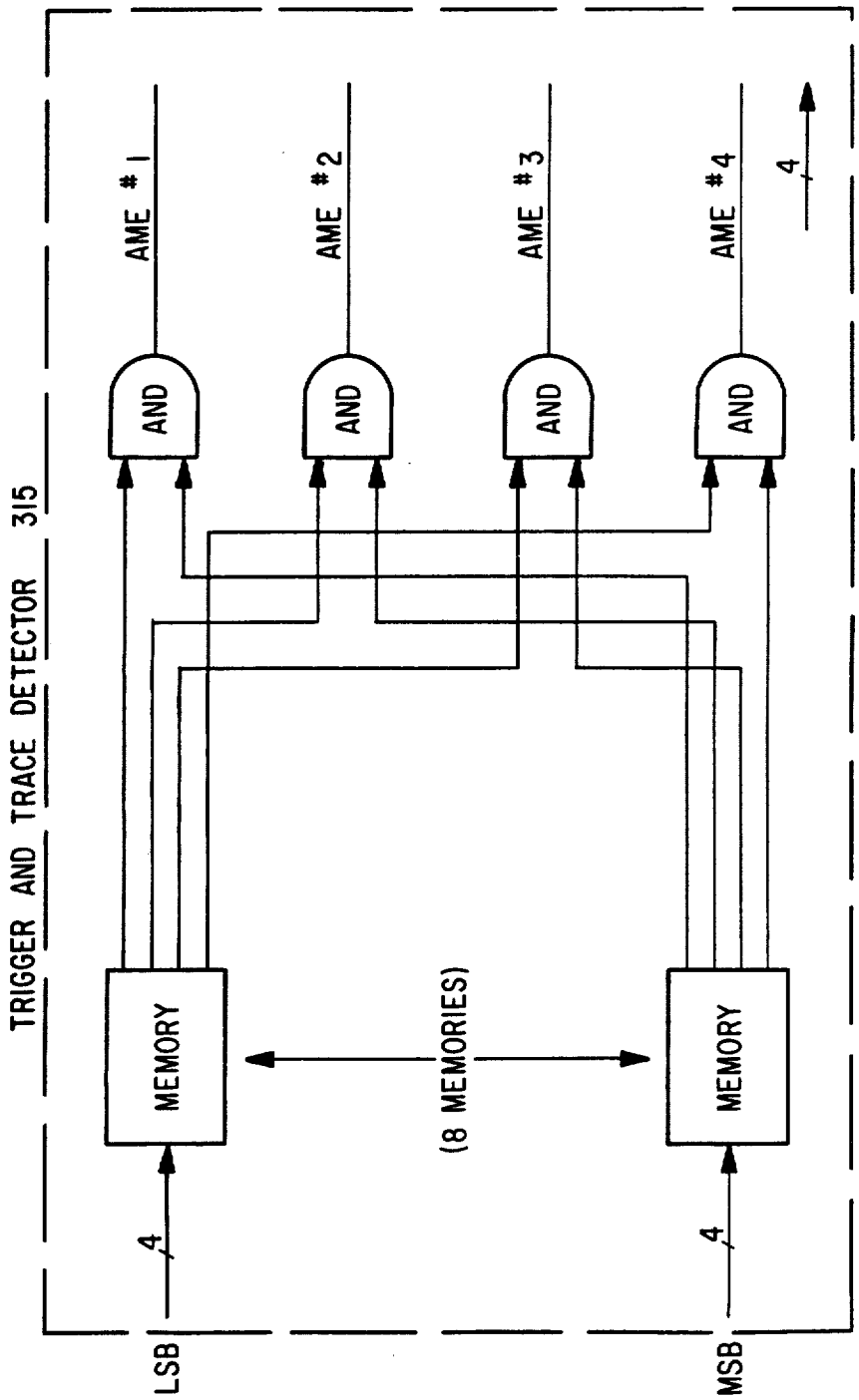

TRIGGER AND TRACE DETECTOR 315
AME #1
AME #2
AME #3
AME #4
AND
AND
AND
AND
4
MEMORY
(8 MEMORIES)
MEMORY
4
4
LSB
MSB

FIGURE 11

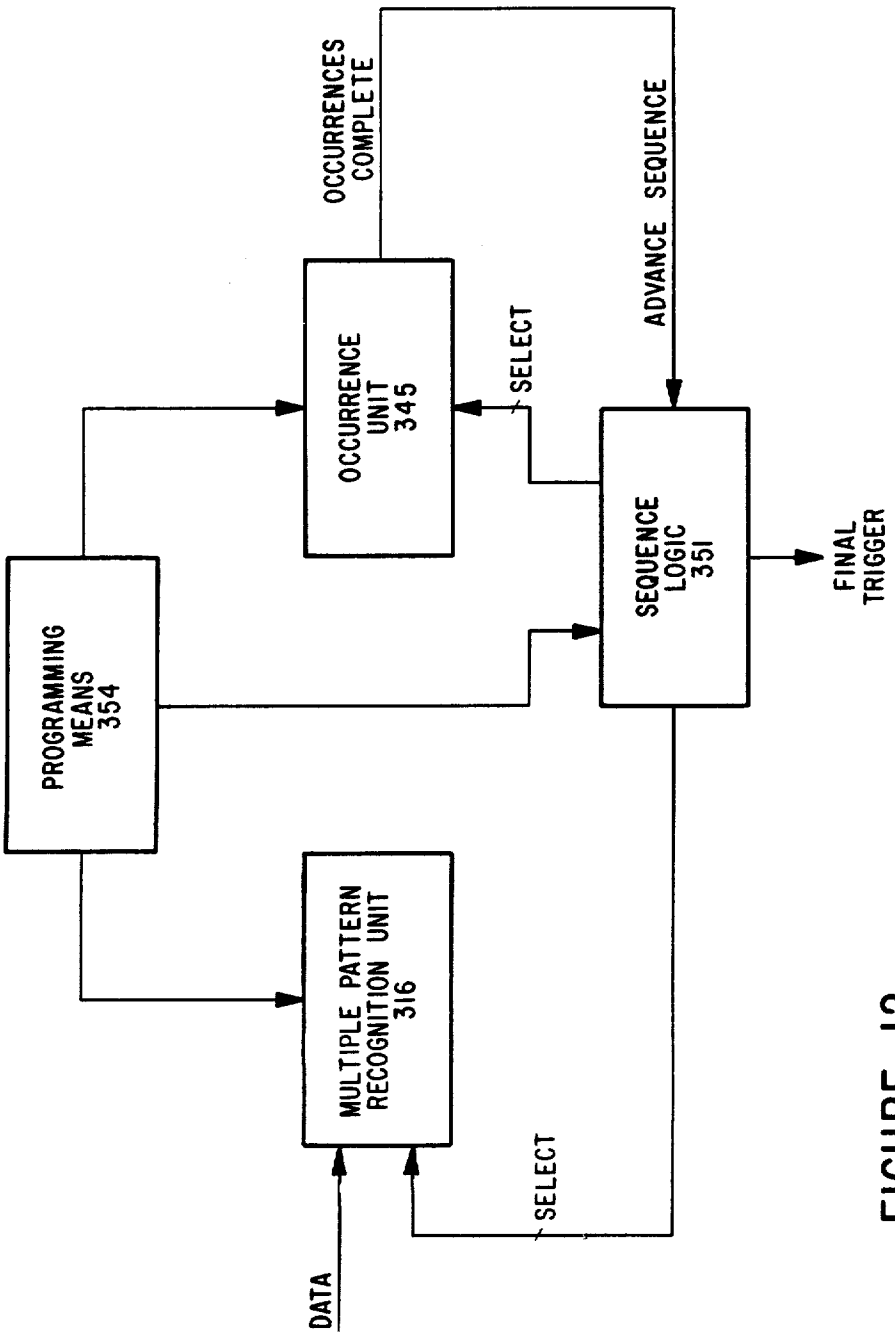

OCCURRENCES COMPLETE
ADVANCE SEQUENCE
OCCURRENCE UNIT 345
SELECT
SEQUENCE LOGIC 351
FINAL TRIGGER
PROGRAMMING MEANS 354
MULTIPLE PATTERN RECOGNITION UNIT 316
SELECT
DATA

FIGURE 12

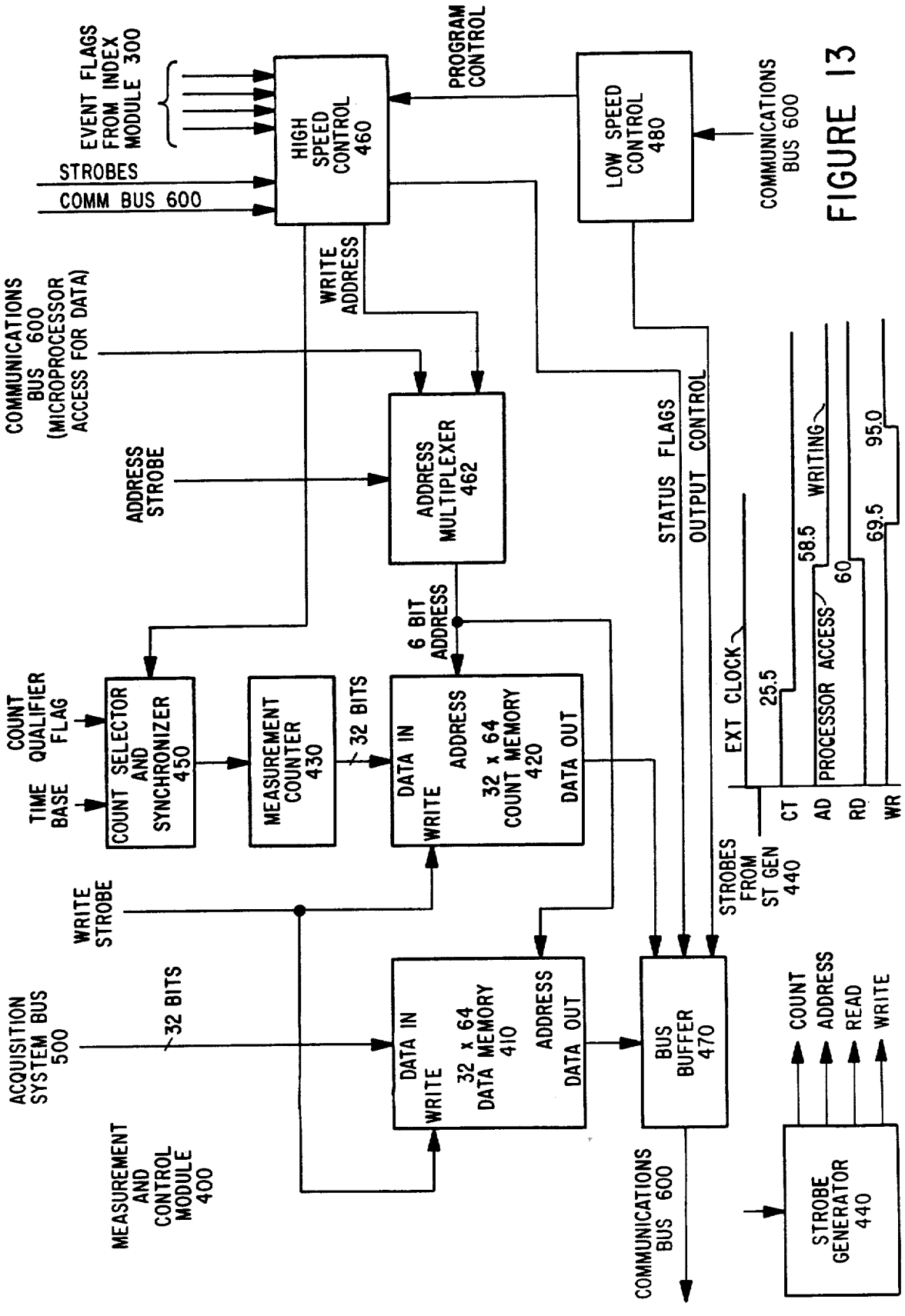

EVENT FLAGS FROM INDEX MODULE 300
STROBES
COMM BUS 600
HIGH SPEED CONTROL 460
PROGRAM CONTROL
LOW SPEED CONTROL 480
COMMUNICATIONS BUS 600
WRITE ADDRESS
COMMUNICATIONS BUS 600 (MICROPROCESSOR ACCESS FOR DATA)
ADDRESS STROBE
ADDRESS MULTIPLEXER 462
STATUS FLAGS
OUTPUT CONTROL
6 BIT ADDRESS
EXT CLOCK
25.5
58.5
WRITING
60
69.5
95.0
PROCESSOR ACCESS
CT
AD
RD
WR
COUNT QUALIFIER FLAG
TIME BASE
COUNT SELECTOR AND SYNCHRONIZER 450
MEASUREMENT COUNTER 430
32 BITS
DATA IN
WRITE
ADDRESS
32 x 64 COUNT MEMORY 420
DATA OUT
STROBES FROM ST GEN 440
WRITE STROBE
ACQUISITION SYSTEM BUS 500
32 BITS
DATA IN
WRITE
32 x 64 DATA MEMORY 410
ADDRESS
DATA OUT
BUS BUFFER 470
COUNT
ADDRESS
READ
WRITE
MEASUREMENT AND CONTROL MODULE 400
COMMUNICATIONS BUS 600
STROBE GENERATOR 440

FIGURE 13

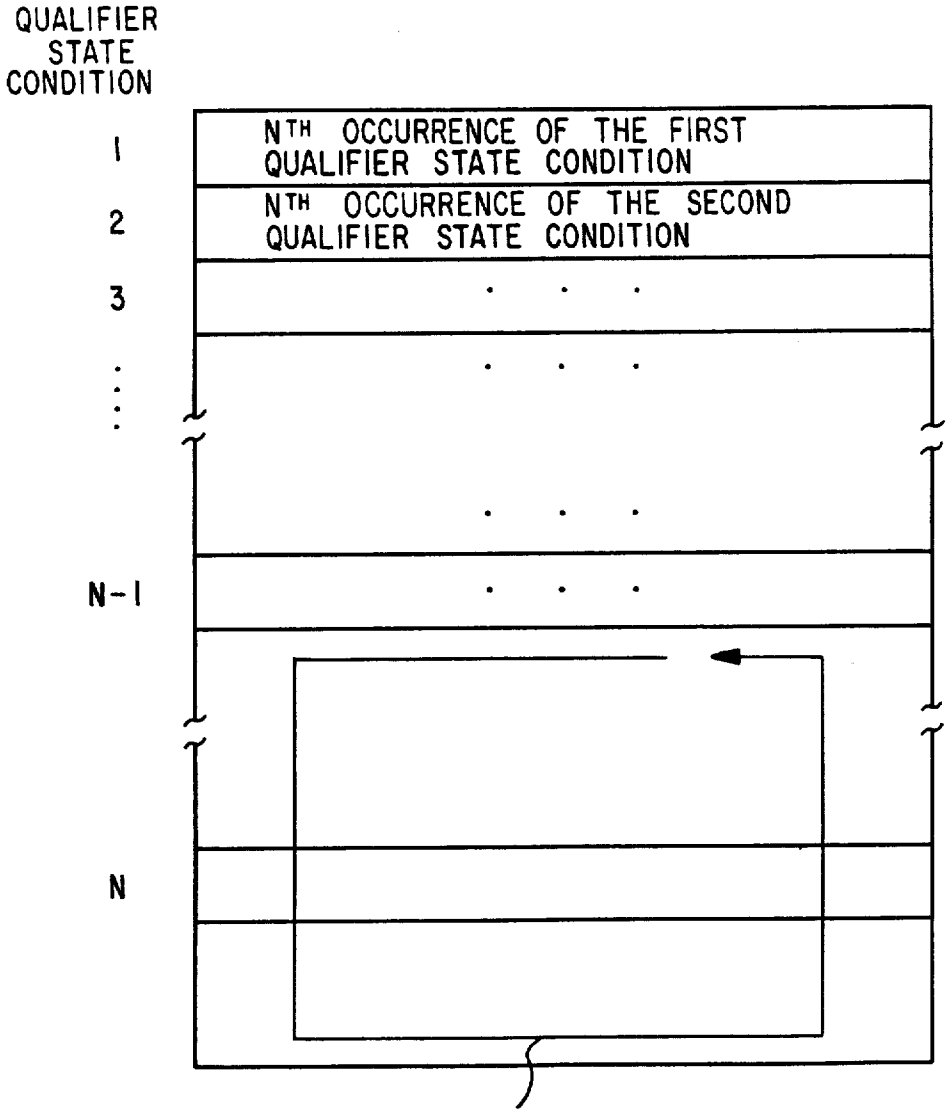

QUALIFIER STATE CONDITION
1
2
3
N-1
N
Nth OCCURRENCE OF THE FIRST QUALIFIER STATE CONDITION
Nth OCCURRENCE OF THE SECOND QUALIFIER STATE CONDITION
SELECTED DATA STATES ARE WRITTEN INTO MEMORY CONTINUOUSLY IN RESPONSE TO THE DETECTION OF THE Nth OCCURRENCE OF THE NEXT TO THE LAST QUALIFYING STATE CONDITION. THE STORAGE LOCATION OF THE SATISFACTION OF THE TRACE SEQUENCE IS IDENTIFIED AND THE DATA STORAGE TERMINATED IN RESPONSE TO THIS EVENT AND THE SELECTED TRACE POSITION (START, CENTER, END)

FIGURE 14

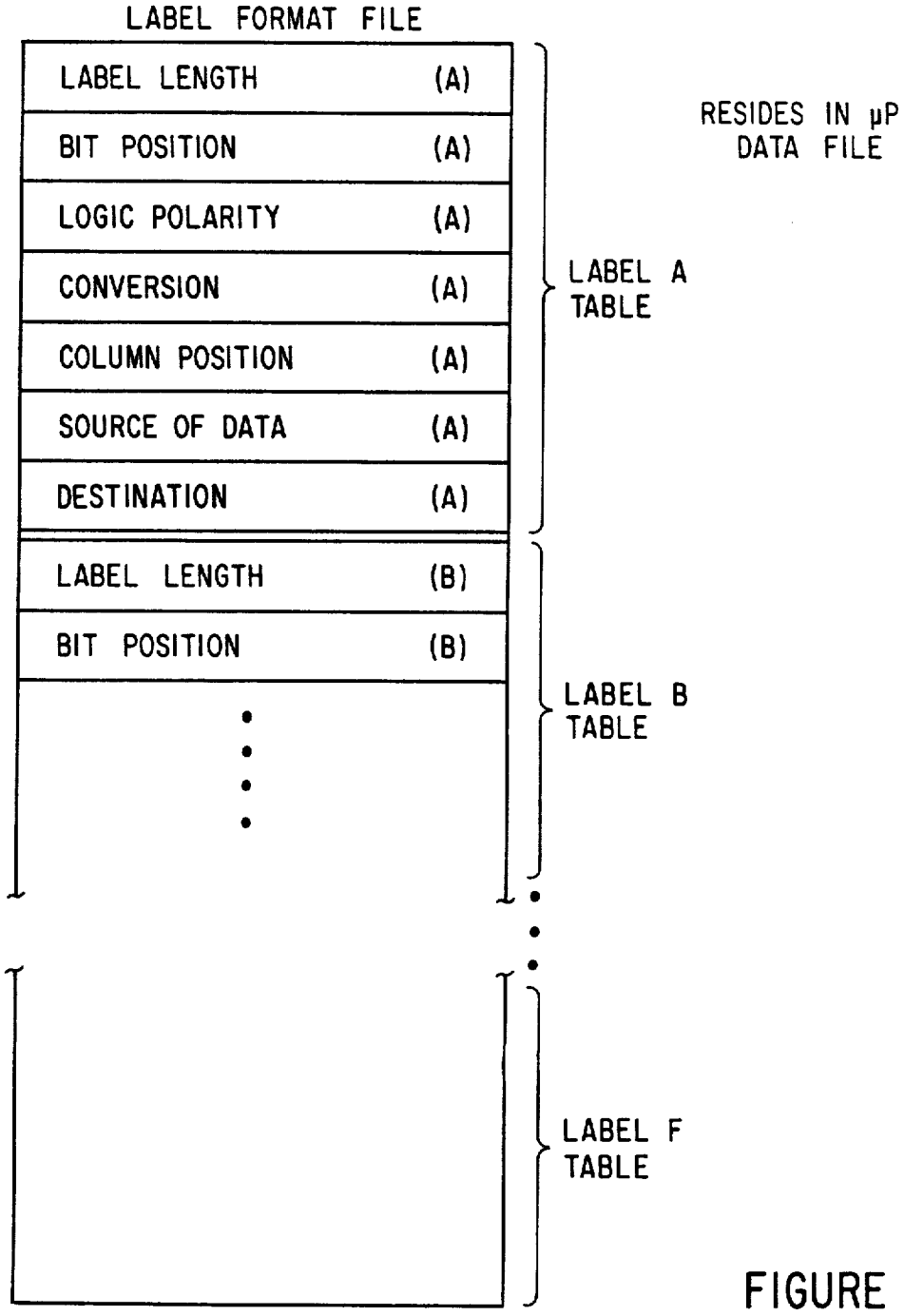

LABEL FORMAT FILE
LABEL LENGTH (A)
BIT POSITION (A)
LOGIC POLARITY (A)
CONVERSION (A)
COLUMN POSITION (A)
SOURCE OF DATA (A)
DESTINATION (A)
LABEL LENGTH (B)
BIT POSITION (B)
RESIDES IN μP DATA FILE
LABEL A TABLE
LABEL B TABLE
LABEL F TABLE

FIGURE 15

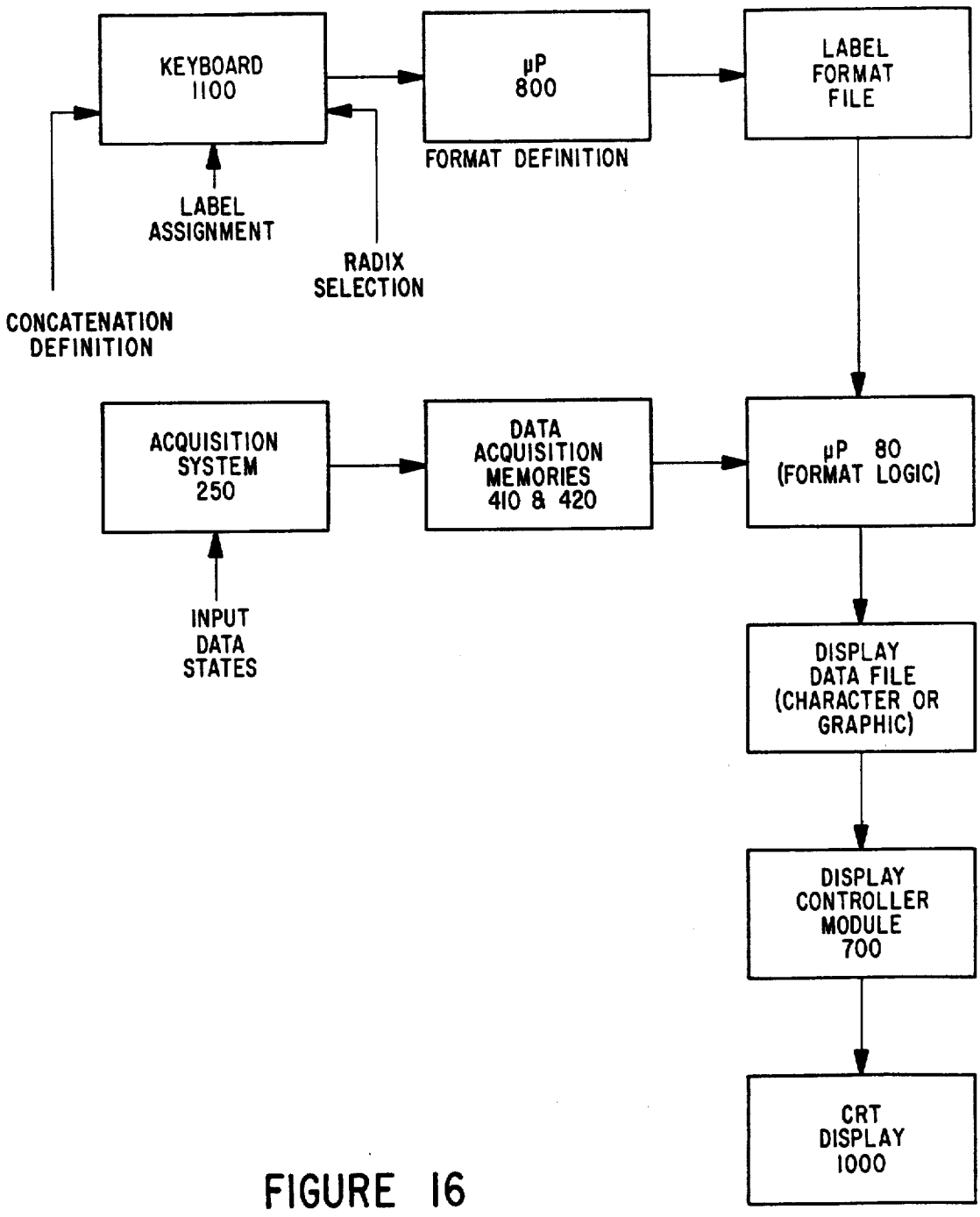

KEYBOARD
1100
μP
800
LABEL
FORMAT
FILE
FORMAT DEFINITION
LABEL
ASSIGNMENT
RADIX
SELECTION
CONCATENATION
DEFINITION
ACQUISITION
SYSTEM
250
DATA
ACQUISITION
MEMORIES
410 & 420
μP 80
(FORMAT LOGIC)
INPUT
DATA
STATES
DISPLAY
DATA FILE
(CHARACTER OR
GRAPHIC)
DISPLAY
CONTROLLER
MODULE
700
CRT
DISPLAY
1000

FIGURE 16

LOGIC STATE ANALYZER WITH FORMAT SPECIFICATION

REFERENCE TO RELATED APPLICATIONS

This application is a division of an earlier filed copending application Ser. No. 210,462, filed on Nov. 25, 1980 by George A. Haag, et al., and amended to be entitled LOGIC STATE ANALYZER WITH STORAGE QUALIFICATION which is now U.S. Pat. No. 4,373,193. That application was contiuation of application Ser. No. 075,787 entitled LOGIC STATE ANALYZER filed Sept. 17, 1979 by the same inventors, and which is now abandoned. That application was in turn a division of a now abandoned application of the same inventors and title, Ser. No. 828,138, filed on Aug. 29, 1977.

The subject matter of the present application is related to the subject disclosed in U.S. Pat. 4,040,025, issued to Justin S. Morrill, Jr., on Aug. 2, 1977, and which was filed on Mar. 31, 1976.

The subject matter of the present application is also related to the subject disclosed in U.S. Pat. No. 4,100,532, issued to William A. Farnbach on July 11, 1978, and which was filed on Nov. 19, 1976.

U.S. Pat. Nos. 4,040,025 and 4,100,532 to Morrill, et al. and Farnbach, respectively, are hereby expressly incorporated by reference.

BACKGROUND AND SUMMARY

Logic state analyzers are used to monitor and record sequences of states that occur in a collection of digital signals in a system under test. A "state" is simply any one of the 2^n logical patterns that n-many digital signals may experience. A sequence of addresses or a sequence of fetched instructions are examples of electrical activity describable as states in a microprocessing environment and that can be monitored by a logic state analyzer to record their "state flow".

To monitor the ongoing sequence of states in a system under test a logic state analyzer samples the electrical values of the signals of interest at times determined by one or more clock signals associated with the system under test. The sampled electrical values obtained are compared to thresholds of selected value and polarity to determine their logical values, each of which will be either true or false, one or zero. Each resulting collection of ones and zeros for a sample is a state in the ongoing sequence of states. It is also simply a binary value that may be stored in a memory. A series of such stored values is a record of the activity occurring in the system under test. Such a record may be termed a trace.

To be useful, a logic state analyzer must produce a trace that bears some desired relation to a specified event. The specification of that relation can be simple or complex, and may involve such notions as storage qualification (i.e., not storing a state as a part of the trace unless some qualifying criteria are met) and sequential triggering. These various relations are set out in a trace specification.

The trace itself is often a tabular listing of captured states. shown in the order in which they appeared. Unless some additional mechanism is at hand, the states in the tabular listing will appear as undifferentiated integer numbers in some radix. For example, if the analyzer received thirty-two digital input signals and displayed each input as either a one or a zero, the trace would consist of a table of thirty-two-bit binary integers. Alternatively, the thirty-two bits could appear as "ten and one half" digit octal or eigth-digit hexadecimal integers. Note that whatever scheme is chosen affects the trace specification; qualification states for storage qualification and the sequence states for a sequential trigger are generally expressed in the same form used to display the states in the trace.

It would be desirable if the user could partition the input digital signals into groups and select an individual radix to be associated with each group. For example, one group of the input digital signals may represent an address most conveniently represented in hexadecimal, while another group may be data best depicted in octal. Still another group may be a collection of miscellaneous status and control lines best seen in binary. It would also be convenient if these groups could be assigned symbolic labels for ease in referring to the groups in the trace and in the trace specification. Such grouping, individual radix selection and labelling is accomplished by equipping a logic state analyzer with a mechanism to receive a format specification. The format specification is a user-determined rule of interpretation for the various input digital signals. It specifies which digital signals belong to the same group, what the associated radix is, and what symbolic label refers to each individual group.

DESCRIPTION OF THE FIGURES

FIG. **1** illustrates the interactive format specification display.

FIG. **2** illustrates the interactive trace specification display.

FIG. **3** illustrates a trace list display of the stored data states.

FIG. **4** illustrates a trace graph display of the stored data states.

FIG. **5** illustrates a trace compare output display list.

FIG. **6** illustrates the input keyboard.

FIG. **7** illustrates a block diagram of the present invention.

FIG. **8** illustrates the distributed memory addressing of the present invention.

FIG. **9** illustrates the relationship between physical and logical addresses of the distributed memory of FIG. **8**.

FIG. **10** is a block diagram of the acquisition system.

FIG. **11** illustrates a multiple pattern recognition unit.

FIG. **12** illustrates a simplified sequential triggering circuit.

FIG. **13** illustrates the measurment and control module.

FIG. **14** illustrates the data format of the data memory.

FIG. **15** illustrates the format of the label format file.

FIG. **16** illustrates the logic flow of the display formatting logic.

FORMAT SPECIFICATION

Data formatting permits the partitioning of **32** input data channels into parameters of interest. Contiguous data channels which behave as a single parameter may be assigned to one of six labels (A–F). For example, in FIG. **1**, illustrating the interactive format specification display, 16 bits of an address bus have been assigned to label "A", 8 bits of a data bus have been assigned to label "D", 1 bit of data on pod **1** has been assigned to label "F", and 7 bits have been left unassigned (labeled

"X"). Further specifications and data manipulations are made by referencing these labels. Each assigned label may be independently declared to have a positive or negative "logic polarity" and converted to an independently selected radix which can be binary, octal, decimal or hexedecimal. Further, the slope of the positive or negative clock transition at which time the input data channels are sampled can be selected ("clock slope").

Keyboard entries to the microprocessor **800**, as shown in FIG. **16**, permit the construction of the label format file, shown in more detail in FIG. **15** which, contains the format specification parameters. This is used to process the stored data states in the construction of the alphabetically cancatenated ASCII display data file and the graphic display data file. Either of the display data files is subsequently selected and used for display purposes by the display control module **700** and the CRT display **1000**.

TRACE SPECIFICATION

The assigned input data channels are sampled at the specified clock transitions and are treated as one sampled state. The trace specification defines which of the sampled states are to be stored for display and which sampled states are to be counted for count measurements. The trace specification comprises a definition of state conditions specifying the trace position, the selective trace, and the count measurement. Each state condition defines a state of the assigned input data channels in any combination of 1's, 0's, and/or X's (dont't care). In octal, decimal or hexedecimal bases the definition is defined in terms of the appropriate alphamumerics and X's.

A trace position may be selected to a start, center or end the selective trace in response to the input data satisfying a predefined state sequence. In this description it will be assumed that the trace position starts the selective trace. A state sequence of up to seven state conditions must be satisfied in a specified order, ignoring intermedate state which do not satisfy the state sequence. The simplest state sequence is a single state condition. Specific segments of branched, looped or nested forms of state flow may be directly located by properly defined state sequences. In addition, each state condition in a state sequence may be required to occur from 1 to 65536 times before the state condition is satisfied. This form of positioning will locate the nth pass of a loop beginning at a given state condition. Clock delay may be incorporated by defining the nth occurrence of any state (an all don't care state specification). The trace logic may also be specified to restart the satisfaction of the predefined state sequence if it is not satisfied before or concurrently with the location of a predetermined restart state condition. A restart on "any state" requires that the state sequence be satisfied without any unspecified intermediate states. For example, FIG. **2** illustrates the interactive trace specification display for a trace position starting upon the satisfaction of **4** state conditions in sequence. A restart state condition is also defined.

The selective trace is a qualification to determine which sampled states will be stored for display. One to seven state conditions may be "OR" specified for collection. Selectively tracing only sampled states of interest elminates the clutter of unnecessary states and magnifies the apparent size of the trace beyond its 64 terms. Also, an occurrence term may be specified so as to store only every nth satisfaction of an "OR" specified state condition. FIG. **2** illustrates the selective trace of every occurrence of a single state condition.

The count measurement performs a "time" of a "state" count associated with each of the (64) states stored and can be displayed in one of two formats:

absolute—the count from the trace position

relative—the count from the previous trace state

The time count is performed by counting the occurrences of an internal clock between sequentially stored states and the display is in the units of seconds. A state count similarly counts the number of occurrences of a specified state condition ("count") between sequentially stored states. For example, specifying "any state" would result in a count of the selected clock transitions of the input data. In FIG. **2**, a state count is performed on the occurrences of a specified state condition intermediate to each sampled state stored.

INTERNAL MEASUREMENT STORAGE

One complete measurement of 64 sampled states, which includes the sampled states satisfying the state conditions defining the state sequence and specifications of the format, trace, and display, may be internally stored. This "current measurement" may be stored or exchanged with a "stored measurement" for later analysis. A "trace compare" mode of operation (described more fully below) compares results of a previously stored trace with the current measurement and may be utilized as a further qualifier on data storage.

DISPLAY SPECIFICATION

The output display format of the current measurement may be selected from a trace list, a trace graph, or a trace compare.

A trace list, illustrated in FIG. **3**, displays a listing of the stored states in their order of occurrence. Twenty trace states, (one per line) are simultaneously presented on the CRT display. The "ROLL" keys allow scanning of the 64 stored states. Each line comprises a line number, the stored state alphabetically sorted into assigned labels in their numerical base, and the time or state count is selected.

A trace graph, as shown in FIG. **4**, presents a graph of the data magnitude of a specified label versus the storage location for all 64 stored states. Each state is given a vertical displacement corresponding to its binary magnitude and an increasing horizontal displacement for successive states in order of their occurrence. The result is a waveform analogous to oscilloscope displays of voltage magnitude. The label to be graphed is selected by specifying the "graphed label". Scaling of state magnitude is controlled by specifying the "upper limit" and "lower limit" on the vertical axis. Limits can be specified directly or dynamically varied with logrithmic autoranging controls. These facilities allow any portion of a graph to be magnified to a full scale presentation. The 20 points corresponding to the lines viewed in the trace list are intensified. The intensified portion also responds to the "ROLL" controls, and their corresponding absolute value may be read in the trace list.

A trace compare as illustrated in FIG. **5** presents a tabular listing of the difference between results in the "current measurement" and the data in the "stored measurement". The listing is formatted and rolled as in the trace list. The results of the two measurements are exclusive OR'ed such that identical corresponding bits are displayed as zeros and unequal bits are displayed as ones. In an octal base a "ϕ3" is equivalent to a binary

"ϕϕϕ ϕ11" and indicates that the right two bits are different in the two measurements. Trace compare also offers a "compared trace" mode which reruns a measurement until the current and stored measurement are either equal or not equal. (STOP =, or STOP ≠) For example, in FIG. **5** of the instrument has rerun trace measurements until the "current measurement" equaled the "stored measurement", as indicated by the "STOP =" specification and revealed by the array of "0"'s in the comparison.

TRACE MODES

Three trace mode options are provided. "Trace" executes a single current measurement. "Continuous trace" repeats the execution of a current measurement continuously. "Compared trace" repeats the execution of a current measurement until the desired comparison with the stored measurement is obtained.

CLOCK ENABLE AND TRIGGER OUTPUTS

A trigger output provides a triggering pulse for external instrumentation such as oscilloscopes. A 50 ns pulse is generated each time the trace position is found. The clock enable output is useful for gating clocks or interrupting the device under test. A high signal level indicates that the instrument is actively searching for the trace position. It remains at the high signal level until the trace position has been found or the halt key is depressed. Both outputs are suspended when the format specification is displayed to allow measurement of channel activity.

KEYBOARD AND SPECIFICATION DESIGNATION

Referring to FIG. **6**, an illustration of the keyboard, the keys are functionally segregrated into four blocks, the "current measurement display", "entry", "edit", and "execute". A power up sequence initially defines a defaul set of sepcifications, displays the default format specification, then automatically selects a hexadecimal trace list display. Activation of the "ROLL DISPLAY" keys permits the presentation of any portion of the 64 states stored. To change the format specification, the "FORMAT SPECIFICATION" key is pressed. The cursor keys in the edit block are used to move the cursor, designating a selectable entry field by a blinking inverse video field on the interactive display.

The trace specification can be edited by selecting the trace specification interactive display by activating the "trace specification" key. Editing is accomplished in the same manner as the format specification is edited. A general description of the functions of the individual keys is given in Appendix A. A detailed description of the interactive display entry fields is given in Appendix B.

DETAILED DESCRIPTION

Input states are sensed through 32 high impedance variable threshold data probes at rates up to 10 MHz. The data probes **100**, illustrated in FIG. **7**, are segmented into four 8 bit data pods and a fifth pod for clock sensing. Each pod may be preset to TTL logic threshold or variably adjusted in the range of +10 to −10 volts to interpret input logic levels.

The 32 input data channels and the clock signal from the data probes **100** are input to the state recognition module **200**. An internal sampling clock is generated in response to the selected clock slope, the input data signals are compared to the selected threshold voltages and interpreted, and the data signals are latched in response to occurrences of the internal sampling clock. The state recognition module **200** outputs the sampled state to the high speed acquisition system bus **500**. The index module **300** accesses the sampled state on the acquisition system bus **500**, compares the sampled state to the selected state conditions and determines the trace position, selective storage events and state count events. The measurement control module **400** also accesses the acquisition system bus **500** and stores state or time counts and sampled data states in response to the events detected by the index module **300**.

The modules of the acquisition system **250** communicate with other system modules via the communications bus **600**, which provides a means for addressing selected modules and for transferring selected data. The entire system functions as a distributed memory, as illustrated in FIG. **8**. For instance, addresses between **1800** and **1FFF** on the communications bus **600** access the state count measurements and the sampled data states stored in the measurement control module **400** memories. FIG. **9** shows another representation of the system architecture, illustrating the relationship between the physical couplings of FIG. **7** and the logical addresses of FIG. **8**.

Referring to FIG. **10**, the index module **300** detects the trace position by first comparing the sampled state on the acquisition system bus **500** with a qualifier state condition stored in the multiple pattern recognition unit **315**. The multiple pattern recognition unit **315** comprises a digital pattern triggering circuit as described in the copending patent application entitled "DIGITAL PATTERN TRIGGERING CIRCUIT", U.S. patent application Ser. No. 743,188 filed Nov. 19, 1976, by William A. Farnbach which is now U.S. Pat. No. 4,100,532. As illustrated in FIG. **11**, the multiple pattern recognition unit **315** comprises 2 pairs of 8 sixteen by four bit memories providing for the detection of up to eight qualifier state conditions, where each qualifier state condition is identified by a 1, 0, X input, format (in binary). Pattern selector **325** of FIG. **10** selects one of the eight lines output from the multiple pattern recognition unit and passes the selected output to the occurrence counter **345**. The occurrence counter **345** counts the occurrences of the selected qualifier state conditions and provides an output in response of counting a specified number of occurrences of the selected qualifier state condition. This output is termed a "break event" and the sequencer logic **350** in response requests the pattern selector **325** to select the next sequential qualifier state condition and requests the occurrence counter **345** to select the corresponding count. The sequencer logic **350** also outputs a "N−1" event flag in response to detection of the occurrence of the "NEXT TO LAST BREAK EVENT". A simplified sequential triggering circuit is illustrated in FIG. **12** where the multiple pattern recognition unit **315** incorporates the functions of the multiple pattern recognition unit **315** and of the pattern selector **325**. The sequence logic **351** incorporates the functions of the sequence logic **350** except that the final trigger is output in response to the completion of the state sequence. Another method of implementing the multiple pattern recognition unit **316** would be to have **3** selector bits be the most significant bits in the address, allowing the comparator to sequence through various segments of memory when comparing sequential state conditions of the state sequence.

Referring again to FIG. **10**, the selective trace is incorporated in a similar manner except that the trace selector **320** of FIG. **10** can "OR" any combination of the AME lines. A trace occurrence counter **340** outputs a trace event flag upon counting each "nth" "ORED" AME event.

The restart unit **310** causes the sequence logic **350** to restart the satisfaction of the state sequence subsequent to the detection of a selected restart state condition. The restart unit is disabled for the data state corresponding to the detection of a break event by sequencer logic **350** which permits the state sequence to be satisfied without any unspecified intermediate state by setting the restart state condition to "any state".

The state count unit **305** strobes a counter in the measurement control module **400** each time the selected state condition to be counted is detected.

The measurement and control module **400** is illustrated in FIGS. **10** and **13**. The event flags from index module **300** are input to the high speed control **460** and determine which sampled states on the acquisition system bus **500** are to be stored. The high speed control **460** addresses the data memory **410** and the count memory **420** accordingly. FIG. **14** illustrates the data format of the data memory **410**. The sampled state conditions resulting in break events are sequentially stored in locations 1 (N−1). Upon detection of the "N−1" event flag, sampled state conditions are sequentially written into the remaining memory locations, writing over the oldest data when the memory is filled. The trace position address of the memory location containing the state condition resulting in the final trigger is stored in a register and sampled states are written into the appropriate number of remaining storage locations. For example, if the trace was defined to end on the detection of the trace portion, no sampled states would be written subsequent to the detection of the trace position. The order of occurrence of the stored data is easily reconstructed by recovery of the trace position address appearing on the communications bus **600** as illustrated in FIG. **8**. Count selector and synchronizer **450** controls the measurement counter **430**, whose contents are stored in count memory **420** upon update of the memory address. The low speed control **480** provides a low speed interface for programming the high speed control **460** and for selecting and latching data for the communications bus **600** interface.

The strobe generator **400**, illustrated in FIGS. **10** and **13**, generates a sequence of strobes which, when coupled with a series of data latches (not shown) and timing logic (not shown) effectuate the orderly performance of machine tasks. In effect, a number of sampled states are simultaneously in various stages of processing at any one time and are "pipelined" through the required logic blocks.

APPENDIX A

GENERAL DESCRIPTION -- KEYBOARD

CURRENT MEASUREMENT DISPLAY

LINES 3 THROUGH 24 ARE DEPENDENT ON THE DISPLAYED MENU CHOSEN, WHICH MAY BE SELECTED BY KEYS IN CURRENT MEASUREMENT BLOCK:

FORMAT SPECIFICATION	SELECT CLOCK SLOPE AND FORMAT 32 CHANNELS INTO LOGICAL LABELS, DESIRED LOGIC POLARITY AND NUMERICAL BASE.
TRACE SPECIFICATION	DEFINE TRACE POSITION, SELECTIVE TRACE AND COUNT MEASUREMENT.
LIST	DISPLAY RESULTANT CURRENT TRACE AND COUNT DATA.
GRAPH	GRAPH RESULTANT CURRENT TRACE DATA FOR SELECTED LABEL. THE 20 INTENSIFIED DOTS CORRESPOND TO TRACE LIST DATA.
COMPARE VS STORE	DISPLAY THE "EXCLUSIVE OR" OF VALID CURRENT DATA WITH VALID STORED DATA, AND SELECT COMPARED TRACE MODE.
ROLL DISPLAY	VIEW TRACE LIST OR TRACE COMPARE DATA. TRACE GRAPH SHOWS INTENSIFIED DOTS THAT
←GRAPH GRAPH →	REPRESENT THE TRACE LIST DATA DISPLAYED.

ENTRY

ALL PROGRAM ENTRIES ARE MADE IN INVERSE VIDEO FIELDS AT THE BLINKING CURSOR, AND MAY BE CHANGED BY THE ENTRY BLOCK OF KEYS:

FIELD SELECT [ ]	ALL FIELDS ENCLOSED WITH BRACKETS [ ] ARE CHANGED BY THIS KEY. THE 1610A SELECTS ONLY ALLOWED CHOICES.
0-9, A-F, X	ALL OTHER FIELDS MAY BE CHANGED USING THESE KEYS.

EDIT

DISPLAYED MENUS MAY BE EDITED BY THE EDIT BLOCK OF KEYS:

DELETE INSERT	USED IN THE TRACE SPECIFICATION MENU ONLY TO OPTIONALLY DELETE OR INSERT STATES TO SPECIFY TRACE POSITION AND SELECTIVE TRACE. A MAXIMUM OF 8 STATES MAY BE USED BETWEEN TRACE POSITION AND SELECTIVE TRACE.
DEFAULT	RETURNS THE DISPLAYED MENU TO A KNOWN (PRESET, TRACEABLE) CONDITION.
INCR DECR	USED IN TRACE GRAPH ONLY TO AUTOMATICALLY CHANGE UPPER OR LOWER GRAPH LIMITS.
← ↑ ↓ →	USED TO MOVE THE BLINKING CURSOR TO A DESIRED FIELD.

EXECUTE

THE REMAINING KEYS ARE THE EXECUTE BLOCK OF KEYS:

CURRENT MEASUREMENT	↓ KEY SAVES CURRENT SPECIFICATION AND DATA MEASUREMENT IN A STORED FILE. THE

APPENDIX A-continued

GENERAL DESCRIPTION -- KEYBOARD	
STORED MEASUREMENT	CURRENT SPECIFICATION AND DATA REMAIN UNCHANGED. ↓ ↑ KEY EXCHANGES THE CURRENT AND STORED MEASUREMENT FILES.
PRINT	PRINTS THE CURRENT DISPLAY, EXCEPT TRACE GRAPH. ON AN HP 9866 LINE PRINTER. TRACE LIST AND TRACE COMPARE WILL PRINT THE CURRENT PAGE AND ANY REMAINING DATA IN MEMORY.
TRACE	EXECUTES THE CURRENT SPECIFICATION, AND IF DISPLAY IS THE FORMAT OR TRACE SPECIFICATION, THE 1610A SWITCHES THE DISPLAY TO TRACE LIST. IF TRACE IS HELD DOWN, THE MEASUREMENT IS TRACED CONTINUOUSLY. IF THE COMPARE TRACE MODE IS SET FOR [STOP=] OR [STOP#] THE MEASUREMENT IS TRACED UNTIL THE CONDITION IS MET. THE INSTRUMENT STATUS (1ST LINE) IS EITHER "COMPARED TRACE-FAILED", (IMPLIES CONDITION NOT MET) OR "COMPARED TRACE-COMPLETE" (IMPLIES CONDITION MET).
STOP	STOPS ANY MEASUREMENT TRACE, COMPARED TRACE OR PRINT IN PROCESS.

APPENDIX B

DETAILED FIELD(S) DESCRIPTION

CLOCK SLOPE:

EXAMPLES: CLOCK SLOPE [+]
CLOCK SLOPE [−]

PURPOSE: TO SELECT THE CLOCK TRANSITION USED T0 STROBE POD DATA INTO THE 1610A.

LABEL ASSIGNMENT AND ACTIVE CHANNELS:

EXAMPLE:

POD4	POD3	POD2	POD1
7------0	7------0	7------0	7------0
AAAAAAAA	AAAAAAAA	DDDDDDDD	XXXXXXXF
!!!!!!!!	!!!!!!!!	!!!!!!!!	!

ACTIVE CHANNELS

PURPOSE: TO ASSIGN LABELS A,B,C,D,E OR F TO ANY NUMBER OF CONTINUOUS CHANNELS INDEPENDENT OF POD BOUNDARIES. IN THE ABOVE EXAMPLE THE LABEL A IS ASSIGNED TO 16 BITS OF POD3 AND POD4, AND MAY REPRESENT A 16 BIT ADDRESS. LABEL D IS ASSIGNED 8 BITS ON POD2 AND MAY REPRESENT AN 8 BIT DATA BUS. LABEL F IS A SINGLE BIT OUALIFIER (READ/WRITE) AND IS ASSIGNED TO THE LEAST SIGNIFICANT BIT ON POD1. ANY UNUSED CHANNELS MAY BE TURNED OFF BY PUTTING AN "X" IN THOSE CHANNELS.

COMMENT: AS MANY AS SIX LABELS OR AS FEW AS ONE MAY BE ASSIGNED ACROSS THE 32 CHANNELS, IF A LABEL IS SPLIT, SUCH AS
AABBBAAA (LABEL IS NOT CONTINUOUS)
THEN AN ERROR MESSAGE "ERROR-SPLIT LABEL"IS DISPLAYED AND THE CURSOR IS LOCKED TO THE LABEL ASSIGNMENT FIELDS UNTIL THE ERROR IS CORRECTED.
PRESSING THE DEFAULT KEY WILL ASSIGN LABEL F TO ALL 32 CHANNELS.
ACTIVE CHANNELS ARE SHOWN BY "!" MARKS FOR EACH ASSIGNED CHANNEL. ABSENCE OF "!" INDICATES LOW CHANNEL (BIT) ACTIVITY, AND IS A GOOD INDICATOR THAT A POD CLIP MAY HAVE FALLEN OFF. CHANNEL ACTIVITY IS NOT DISPLAYED WHILE 1610A IS TRACING.
IF A POD IS CONNECTED TO THE DATA PORT ON REAR OF 1610A, THE CHANNEL ACTIVITY "!" FOR LEAST SIGNIFICANT 2 BITS IS NOT SHOWN (DUE TO SYNCHRONOUS 8 BIT COUNT AND 1610A).

LOGIC POLARITY:

EXAMPLE:

LABEL	A	D	F
LOGIC POLARITY (+, −)	[−]	[−]	[+]

PURPOSE: TO SELECT A LOGIC POLARITY FOR EACH ASSIGNED LABEL.

NUMERICAL BASE:

EXAMPLE:

LABEL	A	B	F
NUMERICAL BASE (BIN, OCT, DEC, HEX)	[HEX]	[OCT]	[BIN]

PURPOSE: TO SELECT A NUMERICAL BASE OF HEXIDECIMAL (HEX), OCTAL (OCT), DECIMAL (DEC), OR BINARY (BIN) FOR EACH ASSIGNED LABEL.

TRACE POSITION:

APPENDIX B-continued

DETAILED FIELD(S) DESCRIPTION

EXAMPLE: [START] TRACE
[CENTER] TRACE
[END] TRACE

PURPOSE: TO SELECT WHETHER THE TRACE STARTS, IS CENTERED OR ENDS UPON A DESIGNATED STATE (WHICH MAY BE CALLED THE TRIGGER STATE). ADDITIONALLY, THE TRIGGER STATE MAY BE DEFINED TO BE A SPECIFIED NUMBER OF OCCURRENCES OF A DESIGNATED STATE.

EXAMPLE:

LABEL BASE	A HEX	OCCUR DEC
FIND IN SEQUENCE	10	00001
THEN	20	00001
THEN	30	00005
[START] TRACE	40	00001
SEQ. RESTART [ON]	50	

COMMENT: THIS EXAMPLE HAS THE FOLLOWING MEANING FOR DEFINING TRACE POSITION:
FIND IN SEQUENCE 00001 OCCURANCE OF STATE 10, THEN THE 00001 OCCURANCE OF STATE 20, THEN THE 00005 OCCURANCE OF STATE 30, AND [START] TRACE AT 00001 OCCURANCE OF STATE 40.
IF DURING THIS SEQUENCE THE RESTART STATE 50 IS ENCOUNTERED BEFORE REACHING THE 00001 OCCURANCE OF STATE 40, THE MEASUREMENT RESTARTS TO AGAIN FIND IN SEQUENCE THE 00001 OCCURANCE OF STATE 10, THEN 00001 OCCURANCE OF STATE 20, ETC.

NOTE:
IF A SEQUENCE STATE IS DEFINED TO BE THE SAME AS THE RESTART STATE, THE SEQUENCE STATE DOMINATES. IF [CENTER] OR [END] WERE SELECTED, SELECTIVE TRACE STARTS AT COMPLETION OF 5 OCCURANCES OF STATE 30 (SEE SELECTIVE TRACE).

SELECTIVE TRACE:

EXAMPLE:

LABEL	A	OCCUR
[ALL STATES]		

PURPOSE: TO TRACE ALL STATES.

EXAMPLE:

	LABEL BASE	A HEX	OCCUR DEC
TRACE			
[ONLY STATE]		6O	00001
OR		7X	
OR		8X	

PURPOSE: TO SELECTIVELY TRACE DESIRED STATES; STATES NOT MEETING THE SELECTION CRITERIA ARE SIMPLY NOT INCLUDED IN THE TRACE.

COMMENTS: THE ABOVE EXAMPLE HAS FOLLOWING MEANING:
DO A SIMULTANEOUS TRACE OF 00001 OCCURANCE OF STATES 60 OR 7X (70 TO 7F) OR 8X (80 TO 8F).

COUNT:

EXAMPLE:

LABEL BASE	A HEX
COUNT [OFF]	
COUNT [STATE]	7X
COUNT [TIME]	

PURPOSE: TO SELECT COUNT MEASUREMENT TO BE [OFF], OR IF ON, TO BE COUNT [STATE] OR COUNT [TIME].

COMMENT: WHEN COUNT IS [OFF], THE TRACE LIST DOES NOT SHOW COUNT DATA FOR THE NEXT TRACE MEASUREMENT.
WHEN COUNT [STATE] IS SELECTED A 32 BIT COUNT OF THE SELECTED STATE 7X (70 TO 7F) IS STORED IN MEMORY WITH EACH POD DATA STATE STORED. THE RESULTANT COUNT DATA IS DISPLAYED IN THE TRACE LIST FOR THE NEXT TRACE MEASUREMENT.
WHEN COUNT [TIME] IS SELECTED A COUNT VALUE OF TIME IS STORED FOR EACH POD DATA STATE STORED IN MEMORY. THE RESULTANT TIME DATA IS DISPLAYED IN THE TRACE LIST FOR THE NEXT TRACE MEASUREMENT

STATE COUNT OR TIME [ABS], [REL]:

EXAMPLE:

LABEL BASE	A HEX		STATE COUNT DEC [ABS]
SEQUENCE	10	–	1043
SEQUENCE	20	–	1033
SEQUENCE	30	–	1023
START	40		0
+01	60	+	20
+02	70	+	30
+03	71	+	31
.	.		.
.	.		.
.	.		.

LABEL BASE	A HEX	STATE COUNT DEC

APPENDIX B-continued

DETAILED FIELD(S) DESCRIPTION

LABEL BASE	A HEX		TIME DEC [REL]
SEQUENCE	10		
SEQUENCE	20		10
SEQUENCE	30		20
START	40		1023
+01	60		20
+02	70		10
+03	71		1
.	.		.
.	.		.
.	.		.

LABEL BASE	A HEX		TIME DEC [ABS]
SEQUENCE	10	–	208.3 US
SEQUENCE	20	–	200.2 US
SEQUENCE	30	–	185.1 US
START	40		.0 US
+01	60	+	80.0 US
+02	70	+	120.9 MS
+03	71	+	122.5 MS
.	.		.
.	.		.
.	.		.

PURPOSE: TO VIEW THE TRACE LIST AND SELECT [ABS] OR [REL] FOR THE STATE COUNT OR TIME DATA.

COMMENTS: WHEN ABSOLUTE [ABS] IS SELECTED THEN EACH STATE COUNT OR TIME IS DISPLAYED IN +/– ABSOLUTE VALUES WITH RESPECT TO THE START STATE 40. ALL STATES BEFORE THE START STATE 40 ARE SHOWN WITH "–" COUNT VALUES. START STATE 40 IS SHOWN AS ALWAYS 0. ALL STATES SHOWN AFTER THE START STATE 40 ARE SHOWN WITH "+" COUNT VALUES.
WHEN RELATIVE [REL] IS SELECTED, THEN EACH STATE COUNT OR TIME IS DISPLAYED SHOWING COUNT VALUES RELATIVE TO THE PREVIOUS STATE COUNT VALUE (IF VALID) WITHOUT SIGN.

GRAPHED LABEL:

EXAMPLE:

GRAPHED LABEL [A]
GRAPHED LABEL [F]

PURPOSE: TO SELECT A DEFINED LABEL A,B,C,D,E, OR F TO BE GRAPHED.

UPPER/LOWER LIMITS:

EXAMPLE:

UPPER LIMIT
177
LOWER LIMIT
000

PURPOSE: TO CHANGE THE UPPER OR LOWER GRAPH LIMITS.

COMMENT: GRAPH LIMITS MAY BE CHANGED USING ENTRY KEYS OR THE LIMITS MAY BE AUTOMATICALLY INCREMENTED OR DECREMENTED USING THE INCR OR DECR KEYS IN THE EDIT BLOCK.
THE UPPER LIMIT MUST BE GREATER THAN LOWER LIMIT, OR ELSE AN "ERROR-OVERLAPPING LIMITS" IS DISPLAYED IN PLACE OF THE GRAPH, WHICH IS NOT DISPLAYED.

COMPARED TRACE MODE:

EXAMPLE:

LABEL BASE	A HEX	COMPARED TRACE MODE [OFF]
SEQUENCE	00	
SEQUENCE	00	
SEQUENCE	00	
START	00	
+01	30	
+02	00	

PURPOSE: TO SHOW THE "EXCLUSIVE OR" OF CURRENT DATA WITH. STORED DATA. ALL ZEROS IMPLIES THAT THE SAME DATA IS IN BOTH FILES, WHILE ANYTHING ELSE (30) SHOWS DATA STATES IN THE TWO TRACES WHICH ARE NOT EQUAL (BITS 4 AND 5, ASSUMING THAT THE LSB IS BIT 0).

EXAMPLE:

LABEL BASE	A HEX	COMPARED TRACE MODE [STOP=]

LABEL BASE	A HEX	COMPARED TRACE MODE [STOP#]

PURPOSE: TO SELECT THE COMPARED TRACE MODE TO BE STOP WHEN EQUAL [STOP=], OR STOP WHEN NOT EQUAL [STOP#].

APPENDIX B-continued

DETAILED FIELD(S) DESCRIPTION	
COMMENTS:	WHEN [STOP=] IS CHOSEN THE MEASUREMENT IS TRACED REPEATEDLY UNTIL THE VALID CURRENT DATA EQUALS THE VALID STORED DATA. THE STATUS OF INSTRUMENT WILL BE "COMPARED TRACE-FAILED" WHICH MEANS THAT THE CURRENT DATA DOES NOT EQUAL THE STORED DATA. THE 1610A THEN TRACES AGAIN SHOWING "COMPARED TRACE-IN PROCESS" AND COMPARES ANOTHER SET OF TRACE DATA. THIS PROCESS CONTINUES UNTIL THE STATUS IS "COMPARED TRACE-COMPLETE" WHICH MEANS THE VALID CURRENT FILE TRACE DATA EQUALS THE VALID STORED FILE TRACE DATA. A SIMILAR OPERATION EXISTS FOR [STOP#], EXCEPT ITS MEASUREMENT CONTINUES UNTIL FILES DO NOT COMPARE.

NOTE:
THIS IS NOT A REAL-TIME MEASUREMENT, BUT RATHER A "SAMPLED COMPARED MODE" THAT IS DEPENDENT IN PART UPON DATA CLOCK RATES AND TRACE SPECIFICATION. THIS MEASUREMENT MODE MUST BE TURNED [OFF] TO OBTAIN THE SINGLE OR CONTINUOUS TRACE MODES.

I claim:

1. Apparatus configurable by a user for selecting, storing and displaying a set of states occurring in a collection of digital signals, the apparatus comprising:

input means having a plurality of inputs coupled to receive the collection of digital signals for performing signal conditioning thereon according to preselected thresholds to produce a collection of conditioned signals;

format specification means for specifying a user selected partition of the plurality of inputs into groups, including means for specifying individual user selected labels each respectively associated with each group, and including means for specifying individual user selected radices each respectively associated with each group;

trace specification means for specifying a set of trace specification state conditions according to which the set of states to be stored and displayed is selected from among the totality of states occurring in the collection of digital signals;

recognition means coupled to the collection of conditioned signals and responsive to the trace specification means for producing control signals indicative of whether or not a state is to be stored;

storage means coupled to the collection of conditioned signals and to the control signals for storing the set of state data selected by the trace specification means; and

display means coupled to the storage means and responsive to the format specification means for displaying the specified labels and including means for displaying according to the specified partition the set of stored state data as groups of integers, each group of integers displayed in its associated radix and each displayed in correlated relation to its associated label.

2. Apparatus as in claim 1 wherein each of the radices can independently be one of hexadecimal, decimal, octal or binary and further wherein the display indicates the radix associated with each label.

3. Apparatus as in claim 2 wherein the trace specification means is responsive to the format specification means by allowing the partition and associated radices specified with the format means to be used in the definition of the trace specification.

4. Apparatus as in claim 1 wherein the trace specification means is responsive to the format specification means by allowing the partition and associated radices specified with the format means to be used in the definition of the trace specification.

5. A method of allowing a user to format a trace of digital signals whose states are collected, stored and displayed by a logic state analyzer, comprising the steps of:

partitioning the digital signals into user selected groups;

assigning a user selected label to each group;

chosing a user selected radix for each group; and

entering into the logic state analyzer a trace specification described in terms of the assigned labels and chosen radices.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,455,624

DATED : June 19, 1984

INVENTOR(S) : George A. Haag et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 62, "states. shown" should be --states, shown--;

Column 2, line 2, "half" digit" should be --half"-digit--;

Column 3, line 30, "dont't" should be --don't--;

Column 3, line 40, "intermedate" should be --intermediate--;

Column 3, line 40, "state which" should be --states which--;

Column 3, line 53, "predetermined" should be --predefined--;

Column 4, line 3, "of a" should be --or a--;

Column 4, line 66, "OR'ed" should be --"OR'ed"--;

Column 6, line 47, "response of" should be --response to--;

Column 6, line 58, "315" should be --316--;

Column 7, line 27, "1 (N-1)." should be --1- (N-1).--;

Appendix A, Columns 9/10, line 7, "GRAPH." should be --GRAPH,--;

Appendix B, Columns 9/10, line 45, "Oualifier" should be --Qualifier--;

Appendix B, Columns 11/12, line 40, "60" should be --60--;

Signed and Sealed this

Twenty-sixth Day of *February 1985*

[SEAL]

Attest:

DONALD J. QUIGG

Attesting Officer *Acting Commissioner of Patents and Trademarks*